WHAT IS CLAIMED IS:

1. A method of decoding a data stream encoded according to a low density parity check (LDPC) code;

wherein the LDPC code is represented by a parity check matrix, in which the rows of the parity check matrix are grouped into subsets in which each column has a maximum column weight of one, and wherein the columns of the parity check matrix correspond to input nodes and the rows of the parity check matrix correspond to parity check sums;

the method comprising the steps of:

receiving a set of input values corresponding to input nodes of the parity check matrix; and

for each subset, repeating a sequence of steps comprising:

for each row of the subset, subtracting a previous check node value from a probability value for each input node contributing to the parity check sum for that row;

generating a new check node value for that row of the subset, using the result of the subtracting step; and

for each input node contributing to the parity check sum for that row, updating a probability value using the new check node value and the result of the subtracting step.

2. The method of claim 1, wherein the parity check matrix is represented by a macro matrix having zero-valued and non-zero-valued entries arranged in block rows and block columns and in which each zero-valued entry corresponds to a q x q zero-valued matrix and each non-zero-valued entry corresponds to a q x q permutation matrix that has at most a single "1" entry in each row and each column and "0" entries elsewhere to define a parity check matrix.

3. The method of claim 1, further comprising:

checking a parity check equation using the estimated probability values.

4. The method of claim 3, wherein the sequence further comprises:

responsive to an instance of the step of checking the parity check equation indicating that current probability values correspond to a true solution, detecting changes in sign of updated probability values.

5. The method of claim 4, wherein the sequence further comprises:

counting a number of rows for which no change in sign is detected by the detecting step; and

responsive to the counting step reaching a selected value prior to an instance of the checking step indicating that current probability values do not correspond to a true solution, outputting a codeword from the current probability values.

6. The method of claim 5, wherein the checking step further comprises:

slicing each probability value to a digital value.

7. The method of claim 1, wherein the received input values have a form corresponding to the ratio of twice a data value to a channel noise term.

8. The method of claim 1, wherein the sequence further comprises:

storing updated probability values in a column sum memory.

9. The method of claim 1, wherein the sequence of steps is repeated for each subset in the parity check matrix, in a first sequence of subsets;

and further comprising:

again repeating the sequence of steps for each subset for each subset in the parity check matrix, in a second sequence of subsets.

10. Decoder circuitry for decoding a received signal stream that was encoded according to a low density parity check (LDPC) code;

wherein the LDPC code is represented by a parity check matrix, in which the rows of the parity check matrix are grouped into subsets in which each column has a maximum column weight of one, and wherein the columns of the parity check matrix correspond to input nodes and the rows of the parity check matrix correspond to parity check sums;

the circuitry comprising:

a check node memory for storing estimates of check node values associated with each of the input nodes over each of a plurality of parity check sums of the LDPC code;

a first adder coupled to the check node memory, for combining a check node value associated with a row of a subset of the parity check matrix with probability value estimates for input nodes participating in the parity check equation for the row corresponding to the check node value, to produce extrinsic estimates;

a parity check update circuit, for updating the check node value using the output of the first adder, the updated estimate of the check node value associated with

the participating input nodes, the output of the parity check update circuit coupled to the check node memory;

a second adder, for adding the extrinsic estimates to the updated estimate of the check node value to produce updated probability values corresponding to the participating input nodes; and

a plurality of bit update circuits, each for storing the updated probability values corresponding to a plurality of input nodes;

routing circuitry, for routing the output of the second adder to the bit update circuits associated with its corresponding input node; and

rerouting circuitry, for routing each updated probability value from the bit update circuits to the first adder.

11. The decoding circuitry of claim 10, wherein the LDPC code is represented by a macro matrix having zero-valued and non-zero-valued entries arranged in block rows and block columns and in which each zero-valued entry corresponds to a p x p zero-valued matrix and each non-zero-valued entry corresponds to a p x p permutation matrix that has at most a single "1" entry in each row and each column and "0" entries elsewhere to define a parity check matrix.

12. The decoding circuitry of claim 10, wherein each of the plurality of bit update circuits comprises a single column sum memory.

13. The decoding circuitry of claim 10, wherein at least one of the plurality of bit update circuits comprises a single column sum memory;

and wherein at least one of the plurality of bit update circuits comprises:

first and second column sum memories; and

circuitry for alternatively coupling the first and second column sum memories to the routing circuitry and rerouting circuitry, respectively.

14. The decoding circuitry of claim 12, wherein each of the plurality of bit update circuits comprises:

an input for receiving initializing estimates for each of the plurality of input nodes.

15. The decoding circuitry of claim 10, further comprising:

a plurality of first adders, in parallel;

a plurality of parity check update circuits, in parallel with one another; and

a plurality of second adders, in parallel with one another;

wherein the check node memory is arranged in data words, each data word storing check node estimates for a plurality of rows of the parity check matrix, each row corresponding to one of the plurality of first adders, a corresponding one of the plurality of parity check update circuits, and a corresponding one of the plurality of second adders.

16. The decoding circuitry of claim 10, further comprising:

a parity check function, for slicing the updated probability values and for evaluating a parity check equation using the sliced updated probability values.

17. The decoding circuitry of claim 16, further comprising:

sign detection circuitry, for detecting changes in sign of the updated probability values; and

a row counter, for counting a number of rows of the parity check matrix over which no change in sign has been detected by the sign detection circuitry.

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